UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,311	09/16/2003	Joy Y. Zhang	TI-36092	2819

23494 7590 12/09/2004

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
CHOE, HENRY	
ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 12/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,311	ZHANG ET AL.	
	Examiner	Art Unit	
	Henry K Choe	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *25-35* is/are allowed.

6)☒ Claim(s) *1,10,17-21,36-38,40 and 41* is/are rejected.

7)☒ Claim(s) *2-9,11-16,22-24 and 39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 10 and 41 are rejected under 35 U.S.C. 102(b) as being anticipated by Butler (Fig. 1).

Butler (Fig. 1) discloses an amplifier circuit comprising an input stage circuit (14) which is configured to receive an input signal (Input) and provide an output signal (output of 14), a pair of output transistors (28, 30) which are configured to provide an output voltage (34), and a controlled resistive circuit (32, 20) comprising at least one controlled resistive element (32) which is coupled to at least one (28 or 30) of the pair of output transistors (28, 30) and wherein at least one controlled resistive element (32) configured to modify a dynamic impedance of the at least one (28 or 30) of the pair of output transistors (28, 30) since the controlled resistive element (32) is connected to the gates of the output transistors 28 and 30.

Claims 17-21, 36-38 and 40 are rejected under 35 U.S.C. 102(b) as being anticipated by Takehara (Fig. 2).

Regarding claims 17 and 36, Takehara (Fig. 2) discloses an amplifier circuit comprising the method steps of sensing (R17) an output voltage (voltage present at the terminal T1) provided by the output stage circuit (Tr5, Tr6), and

modifying (VR1, VR2) a dynamic impedance effect of at least one output transistor (Tr5 or Tr6) of the output stage circuit (Tr5, Tr6) since the output signal of the VR2 is applied to the gate of transistor Tr6 through the R5 and Tr4 and the output signal of the VR1 is applied to the gate of transistor Tr5 through the R2 and Tr3.

Regarding claims 18-21, 37 and 38, the step of modifying (VR1 or VR2) the dynamic impedance comprising using a controlled resistive element (VR1) to add resistance to modify the dynamic impedance effect. It should be noted that the VR1 or VR2 has a capability to operate as an approximately zero resistance during normal operation and increase resistance when the output stage circuit (Tr5, Tr6) approaches the one (+B1 or –B1) of an upper power supply (+B1) and a lower power supply (-B1).

Regarding claim 40, Takehara (Fig. 2) further discloses an amplifier circuit comprising the method step of using a pull down resistor (R16) coupled between the output voltage (voltage present at the terminal T1) and a negative supply voltage (-B1).

Allowable Subject Matter

Claims 2-9, 11-16, 22-24 and 39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for Allowance

Claims 25-35 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: Regarding claims 25 and 31, the closest prior art of record, Takehara (Fig. 2) does not disclose the following limitations: output sense element configured to provide a control voltage for operation of the at least one controlled resistive element.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Patent numbers (3,631,357; 6,316,999) are the differential amplifiers with the push pull output stages.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Henry Choe whose telephone number is (571) 272-1760.

HENRY CHOE
PRIMARY EXAMINER

#951